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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,755	07/30/2003	Takashige Baba	HIRA.0119	6809

38327 7590 11/01/2006

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EXAMINER	
MALKOWSKI, KENNETH J	

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 11/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,755	BABA ET AL.	
	Examiner	Art Unit	
	Kenneth J. Malkowski	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *16 and 17* is/are allowed.

6)☒ Claim(s) *1,2 and 4-15* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 16-17 are allowed. The following is an examiner's statement of reasons for allowance: With respect to claims 16-17, the prior art does not fairly teach the limitation of a data bit signal control circuit that determines usability of n-bit data signals in accordance with the output of a monitoring means, producing a routing control signal wherein the routing control signal is transmitted to the data signal transmission section wherein said transmission section has a clock reproduction selector for selecting a number b of bits from a-bit data signals where a is an integer such that $2 \leq a < n$ and where b is an integer such that $1 \leq b \leq a$ as well as a routing circuit for routing a row of data to be transmitted to the normally operable data signal bits in accordance with the bit routing control signal and in combination with all other limitations disclosed in independent claims 1 and 2.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 4-12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants admitted prior art (hereinafter AAPA) in view of U.S. Patent Application Publication No. 2002/0167897 to Tateno et al.

With respect to claims 1 and 14-15, AAPA discloses a signal communication apparatus 1401, 1402, Figure 14) of the clock reproduction transmission type (1407, Figure 14 is a clock reproduction circuit)) whereby communication is conducted using parallel optical or electrical signals (14051-1405n, Figure 14) the apparatus comprising a data signal reception unit for receiving transmitted data signals (1402, Figure 14), said data signal reception unit (including clock extraction, 1407; phase adjustment 14081-1408n and flip-flops 14091-1409n) comprising: a clock signal extraction/selection circuit for selecting a signals (1407, Figure 14; signal extracted by 1407 is provided to phase adjusters 14081-1408n), n-bit data signals that have been received (signals 14051-1405n), extracting a clock signal from the selected data signal (1407, Figure 14)(applicants specification, and outputting the extracted clock signal as a reference clock signal (page 3 paragraph 3 (clock signal reproduction circuit 1407 extracts a reference clock signal SCK from the data signal Txd1)); a number n of phase adjusting circuits (14081-1408n, Figure 14) for adjusting the phase of the reference clock signal and for producing reproduction clock signals for each of the received n-bit data signals (RCK1-RCKn, Figure 14), the reproduction clock signal providing the timing for redigitization of each data signal (Txd1-Txdn, Figure 14); and a sampling means for redigitizing each of the received n-bit data signals in accordance with the timing provided by the reproduction clock signal for each bit (page 4 paragraph 1 data signal

are synchronized with reproduction clock signals))(applicants specification page 8 paragraph 3 (phase adjusting circuits produce n-bit reproduction clock signals providing the timing of sampling and re-digitization of the data signals. However, AAPA fails to disclose that there are redundant clock reproduction circuits (a clock reproduction circuits) and a clock reproduction selector for selecting a number b of bits from a-bit data signals where a is an integer such that $2 \leq a < n$ and where b is an integer such that $1 \leq b \leq a$. Despite this, clock extraction redundancy which is selected such that there are a redundant clock extractors that select a number b of bits such that $1 \leq b \leq a$ is well known in the art. Tateno, from the same field of endeavor discloses a clock reproduction selector (3-12, Figure 5) for selecting a number b of bits (in this case, 1 bit, the output of selector 3-12) from a-bit data signals (signals from extractor 2-1 and 2-3 that enter selector 3-12, where $a = 2$) where a is an integer such that $2 \leq a < n$ and where b is an integer such that $1 \leq b \leq a$ ($a = 2$, $b = 1$). Therefore, it would have been obvious to one of ordinary skill in the art to implement the clock extraction of a bits and further select b bits of the a extracted bits as taught by Tateno into the optical signal transmission apparatus with n parallel lines as taught by AAPA. The motivation for doing so would have been to reduce frame synchronization loss in frequency and phase (Tateno, page 2 paragraph 22) thereby preventing frame synchronization loss (Tateno, page 2 paragraph 31).

With respect to claim 2, AAPA in view of Tateno discloses the signal communication apparatus according to claim 1, wherein the clock signal

extraction/selection means comprises: a (Tateno: Figure 5, a = 2) first function sections provided for each of the a-bit data signals (Tateno: 2-1, 2-3, Figure 5) of the received n-bit data signals the first function sections constituting a part of a clock signal extraction function (2-1, 2-3 are clock extractors as shown in Figure 5)(page 4 paragraph 88 (clocks of the working and protection system are extracted by clock extractors 2-1 and 2-3); a selection means for selecting b (b = 1) of the a first function sections (3-12, Figure 5); and b second function sections constituting the rest of the clock extraction function and being adapted to output the reference clock signal based on the outputs of the b first function sections (signal from selector 3-12 is used as the reference clock in Figure 5)(Tateno: page 4 paragraph 90 (clock output from selector 3-12 is provided to circuit 5-2)).

With respect to claim 4, AAPA in view of Tateno discloses the signal communication apparatus according to claim 1, wherein the clock signal extraction/selection circuit is provided for each of a blocks (2-1 and 2-3, Figure 5 wherein a = 2) of the received n-bit data signals (AAPA: 1051-105n, Figure 14), and the reference clock signal outputted by the clock signal extraction/selection circuit for each block is distributed to phase adjusting circuits in the block (Tateno: 2-1 and 2-3, Figure 5 wherein a = 2. The selected output of these is sent to a phase alignment for the frame generation unit)(AAPA: Figure 14, selected reference clock is sent to multiple phase adjusters, 14081-1408n in Figure 14)), wherein the clock signal extraction/selection circuit comprises a circuit for switching the reference clock signal (Tateno: 3-12, Figure 5), wherein, in case an abnormality develops in a data signal bit being used for

extracting the reference clock signal for a block and so the clock signals cannot be correctly extracted, the reference clock signal for the block with the abnormality is switched by the switching circuit to a reference clock signal extracted from another block (Tateno: page 4 paragraph 88 (changeover selector mutually changes over clocks of the working system and the protection system respectively extracted by the clock extractors 2-1 and 2-3))(Tateno: page 2 paragraph 21 (changeover operations occur between the working and protection lines if there is a failure in the line being used)).

With respect to claim 5, AAPA in view of Tateno disclose the signal communication apparatus according to claim 1, further comprising an input terminal for a selection signal for changing the selection of the a bits in the clock signal extraction/selection circuit (page 4 paragraph 87 (clock selector 8 selects between clock 1 and clock 2 based on a select signal SEL)).

With respect to claims 6, 8 and 10, AAPA in view of Tateno disclose the signal communication apparatus according to claim 1, further comprising a clock signal monitoring circuit that monitors the voltage level or frequency of the clock signal extracted from the reference clock signal or data signal and which, if it detects abnormality (page 1 paragraph 15 (presence of phase jitter, lack of synchronism between two signals is detected)) in the voltage level or frequency, outputs a control signal for switching the reference clock signal to a normal clock signal extracted from a different data signal bit (Tateno: page 4 paragraph 75 (detection results of 1-3 and 1-6 or by the transmission monitor induce the changeover switch for the changeover from the working clock to protection clock)).

With respect to claims 7 and 9, AAPA in view of Tateno disclose the signal communication apparatus according to claim 6, further comprising a means for indicating the occurrence of an abnormality in the event of detection of an abnormality by the clock signal monitoring circuit (Tateno: page 4 paragraph 75 (detection results of 1-3 and 1-6 or by the transmission monitor induce the changeover switch for the changeover from the working clock to protection clock)). However, AAPA in view of Tateno do not specifically disclose an alarm means for indicating said abnormality. Despite this, creating an alarm is an extremely well known advantageous limitation in any fault detection system. Therefore, it would have been obvious to one of ordinary skill in the art to implement an alarm into the fault detection means as disclosed by AAPA in view of Tateno. The motivation for doing so would have been to create notification that an error has occurred in order to provide possible additional assistance or other error management means.

With respect to claims 11-12, AAPA in view of Tateno disclose the signal communication apparatus according to claim 9 further comprising a circuit for determining a normally operable data signal bit based on the data signal abnormality notifying signal (1-2, 1-5 and 1-3, 1-6 provides a detection result to switch 3-12 Figure 5), and outputting a bit routing control signal designating the manner of routing the data signals to the individual bits (Tateno: page 4 paragraph 75 (detection results of 1-3 and 1-6 or by the transmission monitor induce the changeover switch for the changeover from the working clock to protection clock)).

With respect to claim 13, AAPA in view of Tateno disclose the signal communication apparatus according to claim 12, but do not specifically detail the limitation of a circuit for restoring the data signals of each bit back to the original order of data based on the bit routing control signal. Despite this, circuitry which restores the order of transmitted bits is notoriously well known in the art and is commonplace in data transmission systems. Therefore, it would have been obvious to one of ordinary skill in the art to implement such circuitry for the purpose of being able to retrieve and organize data in a recognizable order. The fact that applicant does not provide an enabling description of the bit restoring circuitry further evidences the fact that such circuitry is well known and obvious in the art. This general circuit is only alluded to one time in the specification on page 11 paragraph 2, "The manner of routing of the data signals...*may* (emphasis added) employ a circuit for restoring the data signal of each bit back to the original order of data in accordance with the bit routing control signal." However, this statement clearly does not enable one of ordinary skill in the art to make and use such a circuit as no details at all are mentioned.

Allowable Subject Matter

4. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following patents are cited to further show the state of the art

with respect to data transmission/ photoelectric conversion and testing apparatuses in general:

U.S. Patent No. 7,039,323 is cited to show one CDR circuit for multiple parallel lines

U.S. Patent No. 6,826,522 is cited to show parallel clock extraction

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth J. Malkowski whose telephone number is (571) 272-5505. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KJM 6/24/06

SUPERVISORY PATENT EXAMINER